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METAL-OXIDE-SEMICONDUCTOR (MOS) DEVICES(U) GEO-CENTERS
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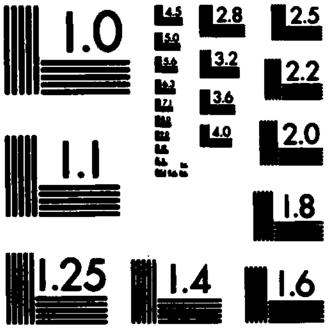
UNCLASSIFIED   N00014-82-C-2361   F/G 20/12   NL


1.0
4.5
5.0
5.6
6.3
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MICROCOPY RESOLUTION TEST CHART
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GC-TR-82-260

EVALUATION OF RADIATION DAMAGE TO METAL-OXIDE-SEMICONDUCTOR (MOS) DEVICES

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GC-TR-82-260

EVALUATION OF RADIATION DAMAGE TO METAL-OXIDE-SEMICONDUCTOR (MOS) DEVICES

PREPARED FOR
THE U.S. NAVAL RESEARCH LABORATORY
WASHINGTON, D.C. 20375
UNDER CONTRACT NUMBER
N00014-82-C-2361

PREPARED BY
GEO-CENTERS, INC.
320 NEEDHAM STREET
NEWTON UPPER FALLS, MA 02164

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DECEMBER 1982

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Introduction

As the metal-oxide-semiconductor (MOS) capacitor emulates the conducting channel of MOSFET and similar device technologies, it is an excellent probe with which to evaluate and predict device performance under various environmental and processing conditions. The physics of the ideal MOS capacitor are well understood, therefore, any deviation from the ideal may be attributed to loss associated with oxide charge, interface states and/or back contact series resistance. Using the MOS capacitor as a probe, the studies conducted at the Naval Research Laboratory involved the theoretical and experimental determination of device performance under varying degrees of ionizing radiation ~~stress.~~ The purpose of these experiments was to provide qualitative and quantitative information on the effects of various hydrogen and nitrogen annealing treatments on the radiation hardness, or resistivity to damage, of MOS capacitors. Toward this end, ~~Geo-Centers, Inc. performed~~ the following tasks:

(1) Construction of capacitor TO-5 packages for device evaluation,

(2) The experimental determination of the 1 MHz capacitance-voltage bias curves for both the pre- and post-irradiated capacitors;

(3) Evaluation of the change in Flat Band Voltage (ΔV_{fb}) for the pre- and post-radiation stressed devices;

(4) Compilation of all 1 MHz data for cataloging purposes and the establishment of a benchmark for the new computer automated test system,

(5) Reported data to the Contracting Officer's Technical Representative (COTR) on a case-by-case basis, as time was of the essence.

MOS Capacitor and Packaging Considerations

The MOS capacitor is a parallel plate capacitor consisting of an evaporated metal gate electrode and a silicon electrode separated by the dielectric, silicon dioxide, SiO_2. The oxide is usually grown thermally, and it is the condition under which it is grown that determines the device's electrical characteristics, radiation sensitivity, and lifetime. Because radiation damage manifests itself in an increase in the density of interface traps (D_{it}), and such increases are measured using capacitance and conductance techniques, it becomes paramount for the accurate evaluation of devices that the loss measured is due solely to the interface states. Process related defects, such as leaky oxides or a non-ohmic or highly resistant contact will distort the capacitance and conductance versus voltage curves, hence information regarding interface trap densities may be obscured. If the back contact series resistance is appreciable (>600 ohms) the predominant loss will occur at the back contact and all information concerning the trap level densities will be unobtainable. In fact, back contact series resistance did present a problem in these studies. Therefore, experiments were performed to evaluate the relative merits of using conducting epoxies versus a gold-chromium eutectic back contact.

For the post-radiation stressed devices, both conducting epoxy and eutectic back contacts produced satisfactory results. In both cases, the loss measured was, as evidenced by a well defined peak in the conductance-voltage curve, predominantly due to the interface traps. However, for the pre-irradiated devices the conducting epoxy back contact proved to be too resistive, and prevented an accurate determination of the density of interface states (by the conductance technique). Subsequent switching to an eutectic bond yielded satisfactory contacts which gave reliable and reproducible measurements of the density of interface states for the pre-stressed devices.

1 MHz Capacitance-Voltage Measurements

The 1 MHz capacitance-voltage curve is one of the most commonly determined measurements for MOS device characterization. The raw data is easily acquired and provides qualitative information concerning the radiation sensitivity of MOS devices. Figure 1 illustrates a typical example of a pre- and post-radiation stressed capacitance-voltage (C-V) curve. The most evident difference between these curves is the large parallel translation of the stressed curve toward negative bias. This is due to an induced positive charge accumulation as a result of exposure to ionizing radiation. In addition to the shift along the voltage axis, the C curve is also stretched out as a result of increased interface state density.

The value of ΔV, the shift of the post-irradiated curve relative to a defined point on the pre-irradiated curve (usually the Flat Band Voltage) is qualitatively indicative of the radiation sensitivity of the device. Experimentally, it had been previously determined that ΔV_{fb} for a given bias, and radiation dose is strongly dependent on processing conditions. Therefore, the evaluation of the change in flat band voltage from the 1 MHz C-V curves becomes an easily accessible parameter with which one may evaluate specific processing conditions towards producing a radiation resistant device.

To evaluate the change in Flat Band Voltage as a function of the process treatment, the following experimental procedures were followed. Forty capacitors were normally chosen, and these, in groups of four, were bonded to a TO-5 header package. The 1 MHz C-V curve was measured for all forty capacitors and the mean Flat Band Voltage was determined for this series of devices. Five TO-5 packages (20 capacitors in all) were then randomly chosen from the group and subjected to a total dose of 1 Megarad (10^6) (from a cobalt-60 source) of ionizing radiation at a fixed bias of -10 volts. Subsequently, the 1 MHz C-V curves were measured on these devices. After all the raw data was collected, the difference in Flat Band Voltage was calculated and tabulated for the 20 irradiated samples. T tests were then applied and the mean and standard deviation of the change in Flat Band Voltage was then determined for this series of devices. Upon tabulation of the ΔV_{fb} values for a series of devices, a correlation of radiation sensitivity and process conditions could then be attempted.

The experimental set-up is as shown in Figure 2. A Boonton L-C, Model 71-A, was used in conjunction with a linear voltage ramp generator and data was recorded on a Hewlett-Packard X-Y recorder. The Boonton meter can measure either the direct or three-terminal effective parallel capacitance of the MOS device from 1-2000 pf. As stray capacitance to ground may be on the order of 50-100 pf, i.e. the same order of magnitude as the DUT itself, the 1 MHz system was configured to measure the three-terminal effective capacitance. The Boonton meter puts out a 15 mv RMS 1 MHz signal, on top of the linearly varying bias voltage, a value well within the small-signal range for most MOS capacitors samples. The accuracy of these meters is quite good being within 0.25% for capacitors with a Q (qualify factor) of 5. Most pre-irradiated samples tested during these experiments had quality factors exceeding 20 at 1 MHz.

While this particular system provided fast data acquisition and analysis, several inadequacies existed which necessitated a more complete analysis of the MOS devices. While comparing the change in flat band voltage for pre- and post-radiation stressed devices provides qualitative information concerning the affects of processing on radiation sensitivity, it fails to provide any accurate quantitative information. Specifically this method fails to yield an accurate number for the density of interface states, lateral nonuniformities, or oxide fixed charge. Also, and equally important, it does not provide any data concerning the spectral location of these traps within the silicon bandgap.

To obtain this information from the high frequency capacitance-voltage data, Terman's analysis is commonly used. The determination of the density of interface states, as a function of the bandgap energy, required first calculating the high frequency capacitance versus surface potential curve. This theoretical curve is then compared to the measured 1 MHz C-V curve and from this comparison a surface potential versus bias voltage curve is derived for the particular device being tested. This resulting curve is then differentiated and the result, $dV_{gate}/d\psi_s$, is then numerically related to the spectral distribution of interface state capacitance.

This technique is obviously involved, and while not necessary, computer processing of the data would certainly expedite the analysis. Unfortunately, Terman's analysis is only sensitive to interface state densities greater than 10^{11} $cm^{-2}ev^{-1}$ while many of the pre-stressed devices were known to have trap levels in the low 10^{11} $cm^{-2}ev^{-1}$ range. This lack of sensitivity points out the second problem with both the qualitative and quantitative capacitance voltage measurement: capacitance is not a sensitive measure of the interface state properties. The measured capacitance of a MOS device depends not only on the interface state capacitance but also the capacitances due to the oxide and the space charge or depletion layer. Therefore, in order to obtain any information regarding the spectral density of interface traps, the contribution from the depletion layer and the oxide capacitances must first be determined and accounted for. This is not true for the measured equivalent parallel conductance of a MOS device. It can be shown that the measured conductance is directly related to the interface state capacitance and thus such measurements are inherently more accurate and sensitive.

While capacitance and conductance may both be measured on an admittance bridge, the current 1 MHz Boonton meter allowed only capacitance measurements. In order to implement the more sensitive and accurate conductance techniques, a new computer automated test system was developed in house by Naval Research Laboratory employees. This system measured capacitance and conductance information, analyzed the data according to various established techniques, and provided analytical information concerning the spectral distribution of interface states. The study of 1 MHz capacitance-voltage data and ΔV_{fb} information provided a benchmark for the evaluation of the performance of the new automated test system. Due to time demands imposed by parallel phases of this program, all data were tabulated and reported separately on a case-by-case basis to the COTR.

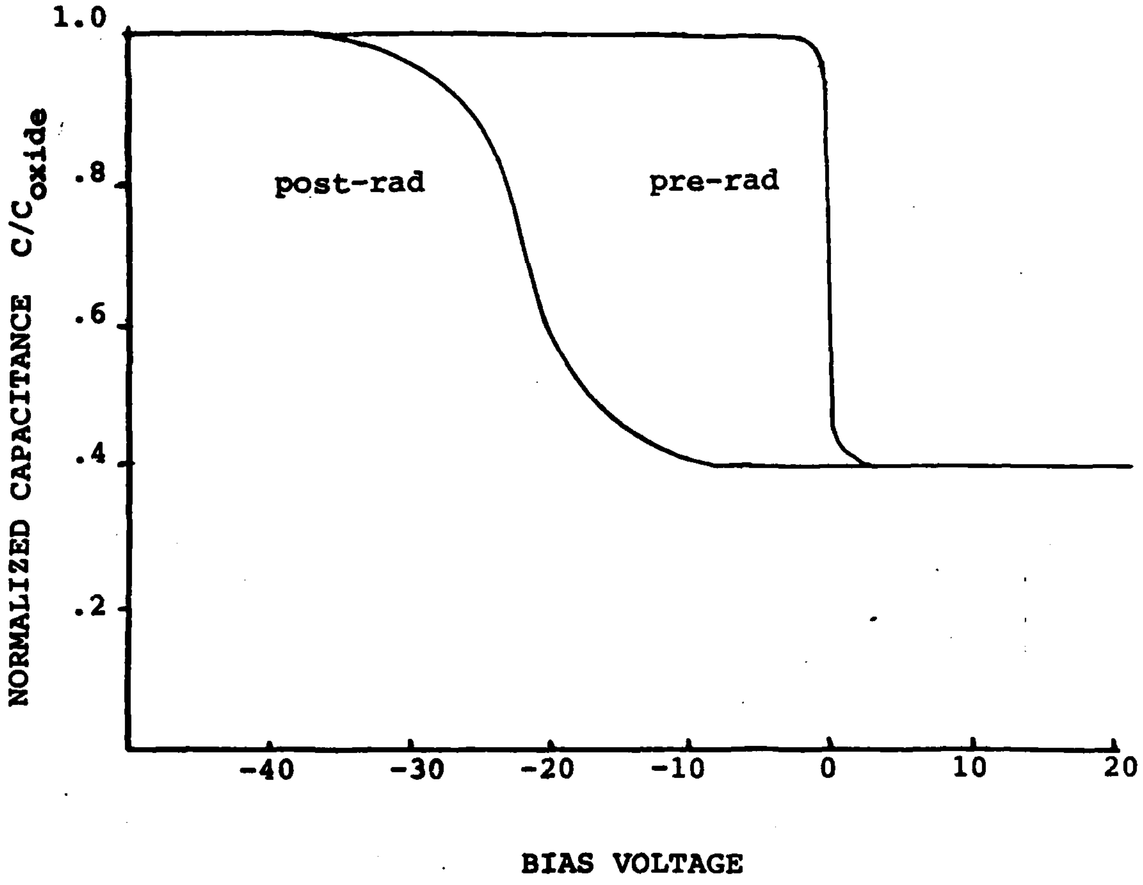

Figure 1 - 1 Megahertz Capacitance - Voltage Curves

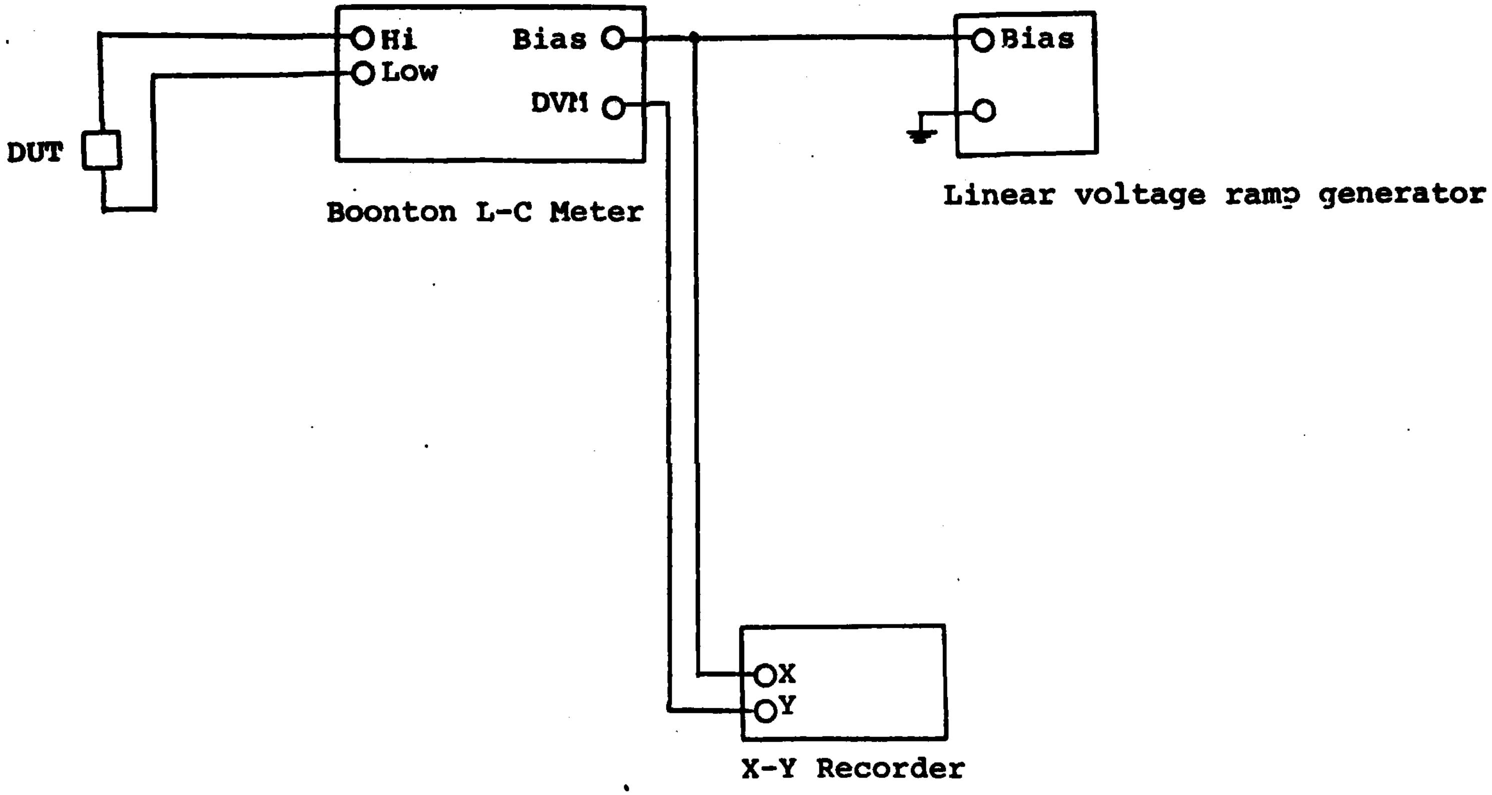
Hi
Low
Bias
DVM
DUT
Boonton L-C Meter
Bias
Linear voltage ramp generator
X
Y
X-Y Recorder

Figure 2 - Boonton 1 Megahertz Capacitance - Voltage Measuring System

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